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10/709,823	06/01/2004	Chc-Hui Chang Chien	13353-US-PA	3822

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JIANQ CHYUN INTELLECTUAL PROPERTY OFFICE
7 FLOOR-1, NO. 100
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TAIPEI, 100
TAIWAN

EXAMINER	
NGUYEN, TANH Q	
ART UNIT	PAPER NUMBER
2182	

NOTIFICATION DATE	DELIVERY MODE
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

USA@JCIPGROUP.COM.TW

Office Action Summary	Application No.	Applicant(s)	
	10/709,823	CHANG CHIEN ET AL.	
	Examiner	Art Unit	
	Tanh Q. Nguyen	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 February 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 June 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Species I (claims 1-9) and cancellation of claims 10-18 (directed to the non-elected species) in the reply filed on February 26, 2007 is acknowledged.

Specification

2. The brackets in the title needs to be removed to read:

INTERFACE AND SYSTEM FOR TRANSMITTING REAL-TIME DATA

Claim Objections

3. Claims 1, 3-4 are objected to because of the following informalities:

"a nonreal time data" in lines 1-2, and "a real-time data" in line 2 of claim 1 should be replaced with --nonreal-time data-- and --real-time data-- respectively

"and the real-time data transmission interface comprising:" in lines 2-3 of claim 1 should be replaced with --the real-time data transmission interface comprising:--

"when the flag state in the flag register is being setting/reading, the 3-state buffer is in an "on" state, while when the flag state is not being setting/reading, and the 3-state buffer is in a high impedance state" in lines 2-4 of claim 3 should be replaced with --wherein when the flag state in the flag register is ~~being~~ setting/reading, the 3-state buffer is in an "on" state, and wherein ~~while~~ when the flag state is not ~~being~~ setting/reading, and the 3-state buffer is in a high impedance state-- for clarity

"and a frequency of the clock signal is 10 MHz" in line 3 of claim 4 should be replaced with --wherein a frequency of the clock signal is 10 MHz-- for clarity

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 2-4 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. The examiner cannot find support for "a control signal latch coupled to the bus interface unit via the internal data bus, wherein **the data output latch** is a latch **for latching a control signal** transmitted by the nonreal-time data interface unit to other units", as recited in lines 11-13 of claim 2.

7. Claim 5 is rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Claim 5 recites "the control logic unit controls the data output latch to latch the nonreal-time data, and determines whether to output the nonreal-time data" in lines 9-10. The limitation "the control logic unit controls the data output latch to latch the nonreal-time data" implies that the nonreal-time data **is outputted**, and the limitation "the control logic...determines whether to output the nonreal-time data" implies that the nonreal-time data **may not be outputted**. One of skilled in the art would not know how to practice the invention with the control unit determining not to output the nonreal-time data, but at the same time controlling the data output latch to latch the nonreal-time data.

8. Claims 8-9 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter, which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. Claim 8 recites "the network interface control unit comprises a programmable interface controller and a TTL/differential level converting interface, wherein the TTL/differential level converting interface is used **to convert**..., and **to cache the real-time data**" in lines 1-5. The claim suggests that the TTL/differential converting interface is used to cache the real-time data. The examiner submits that the TTL/differential level converting interface converts data from one type to another, but does not cache data.

Claim 9 further recites "the sequencer for caching the external condition" in line 7. One skilled in the art would expect a device to cache data, but would not expect the device to cache a condition.

Claim 9 also recites "the real-time data output from the programmable interface

counter" in lines 14. One skilled in the art would expect a counter to output a count value, but would not expect the counter to output real-time data.

9. Claims 2-5, 7-9 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 2 recites "other units" in line 13 and claim 4 recites "other units" in line 3. It is not clear what units are included in "other units" in claim 2 and what other units are includes in claim 4 - as "other units" is already recited in line 7 of claim 2, and as "the other units" is recited in line 9 of claim 2. Clarification is required.

Claim 2 recites an "internal data bus" in line 5 - which suggests a bus for transferring data. Claim 2 also recites "a control signal latch coupled to the bus interface unit via the internal data bus" - which suggests that an internal control bus instead. Clarification is required.

Claim 2 recites "a flag register...for storing a flag state" in the last line. Claim 3 recites "the flag state" in line 2, and in line 3. It is not clear what "a flag state" means. It appears that the flag register is used for storing a flag indicating the state of the tri-state buffer - not the state of a flag.

Claim 5 recites "the data output from the I/O unit" in lines 6-7. There is insufficient antecedent basis for the limitation in the claim.

Claim 5 recites "the control logic unit controls the data output latch to latch the nonreal-time data, and determines whether to output the nonreal-time data" in lines 9-10. The limitation is ambiguous because "the control logic unit controls the data output

latch to latch the nonreal-time data" implies that the nonreal-time data is outputted, and because "the control logic...determines whether to output the nonreal-time data" implies that the nonreal-time data may not be outputted. Clarification is required.

Claim 7 recites "a flag register for storing a flag state" in line 2. It is not clear what "a flag state" means. It appears that the flag register is used for storing a flag indicating the state of the memory unit - not the state of a flag.

Claim 8 recites TTL/differential level on lines 2-3, and on line 3. Claim 8 also recites TTL on line 4. It is not clear what TTL represents as TTL is used throughout the specification without any definition or description.

Claim 8 recites "the network interface control unit comprises a programmable interface controller and a TTL/differential level converting interface, wherein the TTL/differential level converting interface is used to convert..., and to cache the real-time data" in lines 1-5. The claim suggests that the TTL/differential converting interface is used to cache the real-time data, but it is not clear that such interface can cache data.

Claim 9 recites "the sequencer for caching the external condition, which is used by the sequencer for its determining" in lines 7-8. It is not clear how the sequencer can cache a condition, as a condition is not cacheable (only data is cacheable). In addition, there is insufficient antecedent basis for "its determining".

Claim 9 recites "the programmable interface counter" in line 14. There is insufficient antecedent basis for such limitation.

10. The rejections that follow are based on the examiner's best interpretation of the claims.

Claim Rejections - 35 USC § 102

11. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

12. Claim 1 is rejected under 35 U.S.C. 102(b) as being anticipated by Kuver et al. (US 6,438,604).

13. As per claim 1, Kuver teaches a real-time data transmission interface [4, FIG. 2; 4, FIG. 3A] suitable for transmitting nonreal-time data in real-time (data from asynchronous network being transmitted isochronously to a camera [lines 1-8 and last 5 lines of Abstract; FIG. 2]) and transmitting a real-time data in nonreal-time (transmitting isochronous data from a camera to an asynchronous network [lines 1-8 of Abstract; FIG. 2]), the real-time data transmission interface comprising:

a nonreal-time data interface unit [23, FIG. 3A] for receiving/transmitting the nonreal-time data [data from asynchronous network 5, FIG. 3A; col. 7, lines 39-40];

an I/O unit [16, 17, 19 - FIG. 3A; col. 8, lines 41-47] coupled to the nonreal-time data interface unit and being used as a transmission interface for the nonreal-time data and the real-time data (LINK LAYER 16, PCI bridge 19, and DMA 17 interface nonreal-time data from NETWORK CONTROLLER 23 and real-time data from PHYSICAL LAYER 15);

a memory unit ([22, FIG. 3A]; memory from LINK LAYER 16 necessary for

receiving a 1394 (isochronous) data packet from PHYSICAL LAYER 15, and for interpreting the data in the received data packet [col. 9, lines 61-63]) coupled to the I/O unit for caching the nonreal-time data (SDRAM 22 caching nonreal-time data from NETWORK CONTROLLER 23 [col. 12, lines 24-29]) and the real-time data (SDRAM 22 caching real-time data from PHYSICAL LAYER 15 [col. 9, line 26-col. 10, line 6]; memory from LINK LAYER 16 caching real-time data from PHYSICAL LAYER 15 [col. 9, lines 61-63]); and

a network interface control unit [15 - FIG. 3A; col. 8, lines 33-39] coupled to the memory unit for receiving/transmitting the real-time data (receiving the real-time from the camera, or transmitting real-time data to the camera).

Claim Rejections - 35 USC § 103

14. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to

consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

15. Claims 2-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuver et al..

16. As per claims 2-3, Kuver does not teach the nonreal-time data interface unit comprising a data output latch, a data input latch, a control signal latch, and a tri-state buffer - each being coupled to a bus interface unit via an internal bus. Since it was known in the art at the time the invention was made for a nonreal-time data interface unit (i.e. a network controller for asynchronous transmission) to comprise the recited components, with the components being coupled in the manner claimed to facilitate and support efficient data transfer, it would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the nonreal-time data interface unit in the manner claimed, in order to facilitate and support efficient data transfer.

Kuver does not teach a flag register for storing a flag indicating a state for the tri-state buffer. Since it was known in the art to use a flag register to monitor and indicate a state of a tri-state buffer (with the states of a tri-sate buffer being on, off, or high impedance), it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a flag register in order to monitor and indicate the state of the tri-state buffer.

17. As per claim 4, Kuver does not teach the nonreal-time data interface unit to comprise a clock generator for generating and providing a clock signal with a frequency of 10 MHz to other units of the real-time data transmission interface. Since it was

known in the art at the time the invention was made to include a clock generator for generating and providing a clock signal to units of a system in order to synchronize data transfer in the system, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include a clock generator for generating and providing a clock signal in order to synchronize data transfer in the nonreal-time data interface unit. Furthermore, a clock signal with a frequency of 10 MHz is application and technology specific, and no patentability can be accorded to such a specific application or technology.

18. As per claim 5, Kuver does not teach the I/O unit comprising a control logic for controlling read/write operations, a checking circuit for checking an accuracy of output data and generating a checking result in a self test mode, a data output latch for latching nonreal-time data, and a data input latch for latching real-time data. It was known in the art for an I/O unit to comprise the mentioned components and functionalities in order to properly read and write data. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the I/O unit with such components and functionalities, in order to properly read and write data. Kuver further teaches the I/O unit outputting nonreal-time data to nonreal-time data interface unit, and inputting real-time data from the network interface control unit.

19. As per claim 6, Kuver does not teach the memory unit comprising a control unit for controlling the memory unit in accordance with an external control signal, a first address counter for providing a first address, a first memory for storing nonreal-time data, a first buffer latch unit coupled to the first memory via an internal data bus, a

second address counter for providing a second address, a second memory for storing real-time data, and a second buffer latch unit coupled to the second memory via the internal bus.

Kuver teaches a memory unit, hence a memory controller for controlling read/write operations with the memory unit. Since it was known in the art for a memory controller to comprise a control logic unit responding to an external control signal to control a memory unit, an address counter for providing an address in the memory unit for storing data (e.g. Kuver [col. 12, lines 26-29]), and a latch unit for latching the data in the memory unit, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include such components in the memory controller of the memory unit of Kuver in order to control the read/write operations of the memory unit. Furthermore, since Kuver teaches data received from a camera (real time data) and data from the asynchronous network (nonreal-time data) being stored in the memory (see rejection above), Kuver teaches a first memory for storing nonreal-time data and a second memory for storing real time data - hence the invention as claimed.

20. As per claim 7, Kuver does not teach the memory unit comprising a flag register for storing a flag indicating a state of the memory unit. It was known to one of ordinary skill in the art for a memory unit to comprise a flag register storing a flag indicating a state of the memory unit (such as empty and full) in order to use the information in the flag register to prevent overflowing and/or underflowing of the memory unit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to implement the memory unit with a flag register to store a state of the memory unit, in

order to use the information in the flag register to prevent overflowing and/or underflowing.

21. Claims 8-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kuver in view of Christopher et al. (US 5,220,211) and Kosaraju (US 6,907,490).

22. As per claim 8, Kuver does not teach the network interface control unit comprising a TTL/differential level converting interface, wherein the TTL/differential level converting interface is used to convert a type of the real-time data from TTL to differential or in reverse, and to cache the real-time data.

Christopher teaches using a TTL/differential level converting interface [CV1, CV2 - FIG. 2] to convert data from TTL to differential, from differential to TTL, and to cache data [in DRV 20, FIG. 2] - in order to minimize noise radiation [col. 6, lines 14-22; col. 6, lines 27-31; col. 6, lines 48-55]. It would have been obvious to one of ordinary skill in the art at the time the invention was made to incorporate a TTL/differential level converting interface, as is taught by Christopher, in order to minimize noise radiation.

Kuver does not teach the network interface control unit comprising a programmable interface controller. Kosaraju teaches a network interface control unit [physical layer 212, FIG. 2; col. 3, lines 6-7; FIG. 6; FIG. 9] comprising a programmable interface controller [602, 654 - FIG. 6; 902, 924 - FIG. 9] for providing an interface between the network interface control unit and an I/O unit [210, FIG. 2; col. 3, lines 5-6; FIG. 7; FIG. 8] and for controlling routing within the network interface control unit. It would have been obvious to one of ordinary skill in the art at the time the invention was made to include a programmable interface controller, as is taught by Kosaraju, in order

to provide an interface between the network interface control unit and the I/O unit and to control routing within the network interface control unit.

23. As per claim 9, Kosaraju does not teach the programmable interface controller comprising the elements claimed. Since it was known in the art for a conventional programmable controller to include the claimed elements in order to carry out the functionalities of the programmable controller, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the claimed elements in the programmable interface controller to carry out the functionalities of the programmable interface controller.

Conclusion

24. Note that Kosaraju also teaches a memory unit [e.g. 706, FIG. 7] in an I/O unit [link layer - FIG. 7] for caching data received from the network interface control unit [physical layer - FIG. 6], hence providing further support for the memory unit caching real-time data in Kuver.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tanh Q. Nguyen whose telephone number is 571-272-4154. The examiner can normally be reached on M-F 9:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the

Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TANH Q NGUYEN
PRIMARY EXAMINER
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May 9, 2007

TQN
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